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SPECIFICATION

1. Title of the Invention
Semiconductor Integrated Circuit Device
2. Scope of Claims

1. A semiconductor integrated circuit device comprising a polycrystalline silicon or an amorphous silicon formed on an insulating substrate and a field effect transistor using the polycrystalline silicon or the amorphous silicon as a substrate, characterized in that an insulating film of vapor phase growth is formed between the polycrystalline silicon or the amorphous silicon and the insulating substrate.

2. The semiconductor integrated circuit device of claim 1 wherein an SiO_2 film of vapor phase growth is used as the insulating film.

3. The semiconductor integrated circuit device of claim 1 wherein

an Si_3N_4 film of vapor phase growth is used as the insulating film.

4. The semiconductor integrated circuit device of claim 1 wherein the SiO_2 film and the Si_3N_4 film of vapor phase growth are used as the insulating film.

3. Detailed description of the Invention

The present invention relates to a semiconductor integrated circuit device made of a field effect transistor by forming a polycrystalline silicon or an amorphous silicon on an insulating substrate as a substrate.

In recent years, it has been required to develop a large scale integrated circuit device which needs large-sized chip rather than refinement. In such large scale integrated circuit devices, there is no severe demand for their characteristic, however there are some cases having demand firmly for the production yield and cost performance. In that case, a polycrystalline silicon or an amorphous silicon formed on an insulating substrate is used rather than a silicon single crystalline substrate. The so-called integrated circuit device, which includes a built-in thin film transistor, is developed in some industrial fields. It is mainly used in a display device, in particular, it will be used for a liquid crystal display.

In such a large scale integrated circuit device, a large scale and reducing production cost are main subject and also there arises some problems to be obstacle. Most of them are affecting transistor characteristic. Above all leak between source and drain is particularly important problem. The cause of unusual leak phenomenon between source and drain will be described below with reference to an example shown in Figs. 1 and 2.

As shown in Fig. 1, reference numeral 1 shows a glass substrate, 2 shows an N-type polycrystalline silicon, 3 shows a P+ diffusion layer, 4 shows a gate oxide film, 5 shows a polycrystalline silicon electrode, 6 shows a light oxide film, 7 shows a phosphorus glass film, 8 shows an Al wiring, and 9 shows a passivation film. Since thermal treatment is applied to form such device, element of Group 3 or 2 included in a glass substrate 1 is diffused into an N-type polycrystalline silicon, so that a thin P-type polycrystalline silicon 10 is formed. When this layer is formed, it becomes by-pas between P+ diffusion layers of source or drain, and thus leak is generated. The leak occurs by factors such as imperfection of junction caused by existence of the junction in polycrystal, soil, and level, which are fundamental to a factor of generation or dispersion of large leak current.

Fig. 2 shows an example of the case wherein an element in the Group 5 or 6 is included in the glass substrate.

As shown in Fig. 2, reference numeral 11 shows a glass substrate, 12 shows a P-type polycrystalline silicon, 13 shows an N+ diffusion layer, 14 shows a gate oxide film, 15 shows a polycrystalline silicon electrode, 16 shows a light oxide film, 17 shows a phosphorus glass film, 18 shows an Al wiring, and 19 shows a passivation film. As the same with Fig. 1, when thermal treatment is applied, an element of Group 5 or 6 included in the glass substrate 11 is diffused into a P-type polycrystalline silicon to form a thin N-type polycrystalline silicon layer 20. When the layer is formed, it becomes by-pas between N+ diffusion layers of source or drain, which becomes a cause of leak.

The present invention improved the above defect, and it is an object of the invention to prevent an impurity diffusion from an insulating substrate to a polycrystalline silicon or an amorphous silicon, thereby not generating the leak between source and drain, or the like.

The other object of the invention will be clear by the description of the present invention.

The present invention will be described below with reference to an example in Fig. 3.

As shown in Fig. 3, reference numeral 21 shows a glass substrate, 22 shows an N-type polycrystalline silicon, 23 shows a P+ diffusion layer, 24 shows a gate oxide film, 25 shows a polycrystalline silicon electrode, 26 shows a light oxide film, 27 shows a phosphorus glass film, 28 shows an Al wiring, and 29 shows a passivation film. Also, 30 shows an SiO_2 film of vapor phase growth.

As an example of the invention, when an SiO_2 film of vapor phase growth is formed between a glass substrate and a polycrystalline substrate at a thickness of 200 Å to 3000Å, or more, the impurity diffusion into a polycrystalline silicon substrate or an amorphous silicon substrate is prevented by thermal treatment performed in a latter process, and thus the leak is not generated.

According to an example of the invention, the case of using the N-type polycrystalline silicon is described, and also the case of using a P-type polycrystalline silicon or an intrinsic polycrystalline silicon is the same as well as the case of using an amorphous silicon.

Further, an SiO_2 film of vapor phase growth is described as the example of the present invention, however, an Si_3N_4 film of vapor phase growth, a multilayer between the SiO_2 film of vapor phase growth and

the Si_3N_4 film of vapor phase growth, or a film of other vapor phase growth can be used in a similar way.

Furthermore, an example wherein a glass substrate is used as a substrate is described in the present invention, and a ceramic substrate or other insulating film substrate can be used in the same way.

4. Brief Description of the Drawings

Figs. 1 and 2 show cross sectional rough plans of a semiconductor integrated circuit device according to the conventional method.

Fig. 3 shows a cross sectional rough plan of a semiconductor integrated circuit deice according to the present invention.

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